NAMIBIA UNIVERSITY
OF SCIENCE AND TECHNOLOGY

FACULTY OF COMPUTING AND INFORMATICS
DEPARTMENT OF CYBER SECURITY

QUALIFICATION: BACHELOR OF COMPUTER SCIENCE, BACHELOR OF COMPUTER IN CYBER SECURITY & BACHELOR OF INFORMATICS	
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COURSE: COMPUTER ORGANISATION AND ARCHITECTURE	**COURSE CODE**: COA511S
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DURATION: 2H00	**MARKS:** 100

FIRST OPPORTUNITY EXAMINATION QUESTION PAPER	
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THIS QUESTION PAPER CONSISTS OF 5 PAGES
(Excluding this front page)

INSTRUCTIONS

1. Answer ALL the questions on the answer scripts.
2. Write clearly and neatly.
3. Number the answers clearly.

PERMISSIBLE MATERIALS

1. Calculator.

SECTION A [15 MARKS]: Each Question Weighs 1 Mark.

Indicate whether each of the following statements is True or False

1. Organizational attributes include hardware details transparent to the programmer. [True/False]
2. RISC processors are more responsive to interrupts because interrupts are checked between rather elementary operations. [True/False]
3. Machine parallelism exists when instructions in a sequence are independent and thus can be executed in parallel by overlapping. [True/False]
4. Addition and subtraction can be performed on numbers in two's complement notation by treating them as unsigned integers. [True/False]
5. Although convenient for computers, the binary system is exceedingly cumbersome for human beings. [True/False]
6. In the Direct Memory Access (DMA) mode, the I/O module and main memory exchange data directly, without processor involvement. [True/False]
7. Paging is usually visible to the programmer and is provided as a convenience for organizing programs and data and as a means for associating privilege and protection attributes with instructions and data. [True/False]
8. It is not possible to connect I/O controllers directly onto the system bus.[True/False]
9. Binary notation is more compact than hexadecimal notation. [True/False]
10. In a system without virtual memory, the effective address is a virtual address or a register. [True/False]
11. The SRAM is the building block for level 1 Cache memory. [True/False]
12. Interrupt is one of the five states for a process. [True/False]
13. Instruction pipelining is a powerful technique for enhancing performance but requires careful design to achieve optimum results with reasonable complexity. [True/False]
14. The XOR operator yields false if both its operands are true. [True/False]
15. The AGP expansion cards found on the on the motherboard are superior to PCI Express (PCIe). [True/False]

SECTION B [15 MARKS]: Each Question Weighs 1 Mark.

Choose the correct for each of the following:

1. In an optical CD, the areas between pits are called _____.

   A. lands B. sectors

   C. cylinders D. strips

2. A variety of errors can occur while a computer system is running. When that happens, the OS must make a response that clears the error condition with the least impact on running applications. The OS takes care of these errors through the _____ service.

   A. Error correction and response B. Error correcting

   C. Error responsiveness D. Error detection and response

3. An extendable precision format is a format with a precision and range that are defined under _____.

   A. system control B. program control

   C. user control D. shadow control

4. In floating-point arithmetic, when a positive exponent exceeds the maximum possible exponent. It is known as _____.

   A. Exponent underflow B. Exponent overflow

   C. Significand underflow D. Significand overflow

5. Which properties do all semiconductor memory cells share?

   A. They exhibit two stable states which can be used to represent binary 1 and 0

   B. They are capable of being written into to set the state

   C. They are capable of being read to sense the state

   D. All of the above

6. In any number, the leftmost digit is referred to as the _____.

   A. lease significant digit B. a most common digit

   C. most significant digit D. least common digit

7. A _____ is a mechanism that provides for communication among CPU, main memory, and I/O.

   A. system interconnection B. CPU interconnection

   C. peripheral D. processor

8. The _____ determines the opcode and the operand specifiers.

A. decode instruction B. fetch operands

C. calculate operands D. execute instruction

9. A _____ is a dispatch able unit of work within a process that includes a processor context and its own data area for a stack.

A. Process B. Process switch

C. Thread D. Thread switch

11. The _____ determines the opcode and the operand specifiers.

A. decode instruction B. fetch operands

C. calculate operands D. execute instruction

10. The _____ is the processor memory responsible for facilitating performance of a processor

A. DDR3 B. DDR2

C. DDR4 D. Level 2 cache

12. Which of the following interrelated factors go into determining the use of the addressing bits?

A. number of operands B. number of register sets

C. address range D. all of the above

13. The most fundamental type of machine instruction is the _____ instruction.

A. conversion B. data transfer

C. arithmetic D. logical

14. _____ are used in digital circuits to control signal and data routing.

A. Multiplexers B. Program counters

C. Flip-flops D. Gates

15 . A line includes a _____ that identifies which particular block is currently being stored.

A. cache B. hit

C. tag D. locality

SECTION C [70 MARKS]: Comprehension questions.

Question 1

a) Outline any four (4) distinctive features or characteristics of generation one (mid 1940s) of computers (4 marks)

b) List and briefly describe the four CPU key components (4 marks)

c) I/O (Input/Output) is an information processing system designed to send and receive data from a computer hardware component, device, or network. Data can be sent between devices over a network . List and discuss any 4 types of computer Input /output strategies (8 marks)

Question 2

a) Use a clearly labelled diagram to describe the relationship between computer memory size, speed and coast. (5 marks)

b) List and briefly describe the four CPU registers that are essential to instruction execution (8 marks)

c) In computing, cache replacement policies (also frequently called cache replacement algorithms) are optimizing instructions, or algorithms, that a computer program or a hardware-maintained structure can utilize in order to manage a cache of information stored on the computer. . List and briefly describe three cache replacement policies (6 marks)

Question 3

a) Discuss CISC and RISC Architecture under the following themes by ticking (V)which applies (6 marks)

	Theme	**RISC**	**CISC**	**Marks**
i	Instruction take Single clock cycle			1
ii	Hardware centric			1
ii	More efficient Use of RAM			1
iv	Variable length Instruction			1
v	Provide 2 examples of each (CISC & RISC)	*(any two)*	*(any two)*	4

b) Among other factors, computer performance is guided by two famous laws, the Moore's law (1965) and Amdal's law(1967). State these laws(you may use your own words). (4 marks)

Question 4

The Main Memory consist of 8 GB, and suppose this memory is word addressable meaning that every word has its own unique address for accessing it. (9 marks)

a) Compute the number of addressable words in this memory (4 marks)

b) Suppose this memory is divided into fixed length of 256 words each
How many blocks are in this memory? (3 marks)

c) How many lines of cache memory will be required to accommodate all blocks of main memory in (b) above by using the direct cache addressing scheme? (2 marks)

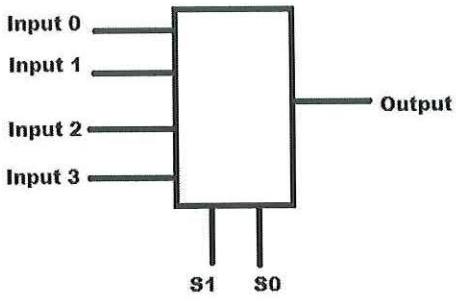
Question 5

a) Give any two examples of each of the following types of digital circuits (4 marks)

i) Combinational
ii) Sequential

b) Identify(name) the following important combinational circuit found in the CPU (2 marks)

c) What is the role of S1 and S2 in this circuit? (2 marks)



d) Draw a truth table depicting the circuit above. As shown in the diagram above your truth table should include two inputs and one outputs. (8 marks)

*****END OF PAPER*****